CLAIMS

What is claimed is:

1. A DC coupled class AB transconductance block, comprising:

first DC coupled transconductance stage operably coupled to produce a first differential current from a differential input voltage based on a first bias voltage;

second DC coupled transconductance stage operably coupled to produce a second differential current based on the differential input voltage and a second bias voltage, wherein output current of the class AB voltage current converter is a sum of the first differential current and the secondary differential current; and

biasing circuit operably coupled to produce the first bias voltage and the secondary bias voltage, wherein the first bias voltage is greater than the secondary bias voltage.

2. The class AB voltage to current converter of claim 1, wherein the first transconductance stage further comprises:

first DC coupled transistor operably coupled to receive a combination of a first leg of the differential input voltage and the first bias voltage; and

second DC coupled transistor operably coupled to receive a combination of a second leg of the differential input voltage and the first bias voltage, wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the first differential current and the second transistor produces a second leg of the first differential current.

3. The class AB voltage to current converter of claim 1, wherein the second transconductance stage further comprises:

first DC coupled transistor operably coupled to receive a combination of a first leg of the differential input voltage and the secondary bias voltage; and

second DC coupled transistor operably coupled to receive a combination of a second leg of the differential input voltage and the secondary bias voltage, wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current.

4. The class AB voltage to current converter of claim 3 further including a third transconductance stage, the third transconductance stage further comprising:

first DC coupled transistor operably coupled to receive a combination of a first leg of the differential input voltage and the secondary bias voltage; and

second DC coupled transistor operably coupled to receive a combination of a second leg of the differential input voltage and the secondary bias voltage, wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current.

5. The class AB voltage to current converter of claim 4 further including a fourth transconductance stage, the fourth transconductance stage further comprising:

first DC coupled transistor operably coupled to receive a combination of a first leg of the differential input voltage and the secondary bias voltage; and

second DC coupled transistor operably coupled to receive a combination of a second leg of the differential input voltage and the secondary bias voltage, wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current.

6. The class AB voltage to current converter of claim 5 further including a fifth transconductance stage, the fifth transconductance stage further comprising:

first DC coupled transistor operably coupled to receive a combination of a first leg of the differential input voltage and the secondary bias voltage; and

second DC coupled transistor operably coupled to receive a combination of a second leg of the differential input voltage and the secondary bias voltage, wherein the second transistor is operably coupled to the first transistor such that the first transistor produces a first leg of the secondary differential current and the second transistor produces a second leg of the secondary differential current.

7. The class AB voltage to current converter of claim 1, wherein the biasing circuit further comprises a reference current source operably coupled to a current mirror to produce a bias signal.

8. The class AB voltage to current converter of claim 1, wherein the biasing circuit further comprises:

first reference voltage source operably coupled to produce the first bias voltage;

second reference voltage source operably coupled to produce the secondary bias voltage;

first resistive pair operably coupled to provide the first bias voltage to the first transconductance stage; and

second resistive pair operably coupled to provide the secondary bias voltage to the secondary transconductance stage.

9. The class AB voltage to current converter of claim 1 further comprises:

third transconductance stage operably coupled to produce a third differential current based on the differential input voltage and a third bias voltage, wherein output current of the class AB voltage current converter is the sum of the first differential current, the second differential current, and the third differential current, wherein the biasing circuit produces the third bias voltage, wherein the second bias voltage is greater than the third bias voltage.

10. The class AB voltage to current converter of claim 9 further comprises:

fourth transconductance stage operably coupled to produce a fourth differential current based on the differential input voltage and a fourth bias voltage, wherein output current of the class AB voltage current converter is the sum of the first differential current, the secondary differential current, and the third differential current, and the fourth differential current wherein the biasing circuit produces the fourth bias voltage, wherein the third bias voltage is greater than the fourth bias voltage.

11. The class AB voltage to current converter of claim 10 further comprises:

fifth transconductance stage operably coupled to produce a fifth differential current based on the differential input voltage and a fifth bias voltage, wherein output current of the class AB voltage current converter is the sum of the first differential current, the second differential current, the third differential current, the fourth differential current and the fifth differential current, wherein the biasing circuit produces the fifth bias voltage, wherein the fourth bias voltage is greater than the fifth bias voltage.

12. A DC coupled class AB transconductance block, comprising:

first DC coupled transconductance stage operably coupled to produce a first differential current from a differential input voltage based on a first bias voltage;

second DC coupled transconductance stage operably coupled to produce a second differential current based on the differential input voltage and a second bias voltage, wherein output current of the class AB voltage current converter is a sum of the first differential current and the secondary differential current;

biasing circuit operably coupled to produce a bias current;

a resistor ladder comprising a plurality of resistors wherein at least one resistor is coupled between each transconductance stage of the DC coupled class AB transconductance block;

wherein each transconductance stage is biased to a different voltage level relative to all other transconductance stages; and

wherein an output transconductance signal is a sum of each of the transconductance signals produced by each of the transconductance stages.

13. The DC coupled class AB transconductance block of claim 12 further comprising a third transconductance stage.

14. The DC coupled class AB transconductance block of claim 13 further comprising a third transconductance stage.

15. The DC coupled class AB transconductance block of claim 14 further comprising a fourth transconductance stage.

16. The DC coupled class AB transconductance block of claim 15 further comprising at least five transconductance stages.

17. A radio frequency (RF) transceiver integrated circuit, comprising:

a local oscillator that generates an RF local oscillation signal corresponding to an RF channel;

a receiver section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the receiver section receives an incoming RF signal, and wherein the receiver section down-converts the incoming RF signal based upon the RF local oscillation signal to produce an incoming baseband signal;

a transmitter section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the transmitter section receives an outgoing baseband signal, and wherein the transmitter section up-converts the outgoing baseband signal to produce an outgoing RF signal; and

wherein the local oscillator further comprises a phase locked loop that generates a phase locked loop oscillation signal that further comprising a multi-stage transconductance block for producing a linearized transconductance current as a part of converting a voltage to a current in a mixing stage of the phase locked loop.

18. In a Radio Frequency (RF) transceiver mixer module, a method for down-converting a received RF signal, comprising:

receiving the RF signal at an input of a transconductance block;

producing a linearized transconductance signal within a mixing stage of a phase-locked loop;

mixing the linearized transconductance signal with a local oscillation;

producing one of a down converted signal to a baseband processor or an upconverted RF signal for transmission from an antenna.

19. A radio frequency (RF) transceiver integrated circuit, comprising:

a local oscillator that generates an RF local oscillation signal corresponding to an RF channel;

a receiver section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the receiver section receives an incoming RF signal, and wherein the receiver section down-converts the incoming RF signal based upon the RF local oscillation signal to produce an incoming baseband signal;

a transmitter section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the transmitter section receives an outgoing baseband signal, and wherein the transmitter section up-converts the outgoing baseband signal to produce an outgoing RF signal; and

wherein the local oscillator further comprises:

a phase locked loop that generates a phase locked loop oscillation signal; and

a mixing stage that receives phase the locked loop oscillation signal and the phase locked loop oscillation signal, wherein the mixing stage further includes:

a transconductance block that includes a plurality of transconductance stages for producing a linearized current as a function of an input signal;

mixing circuitry for mixing the linearized current with a local oscillation to produced a linearized mixed output current signal; and

an output stage coupled to the drain terminal of the mixing circuitry to convert the linearized mixed output current signal to a voltage signal.

20. The RF transceiver integrated circuit of claim 19 wherein the transconductance block comprises at least three transconductance stages for producing linearized output currents that are summed.

21. The RF transceiver integrated circuit of claim 19 wherein the transconductance block comprises five transconductance stages for producing linearized output currents that are summed.